

RETICLE SET, METHOD FOR DESIGNING A RETICLE SET, EXPOSURE
MONITORING METHOD, INSPECTION METHOD FOR RETICLE SET AND
MANUFACTURING METHOD FOR A SEMICONDUCTOR DEVICE

5 CROSS REFERENCE TO RELATED APPLICATIONS

This application is based upon and claims the benefit of
priority from prior Japanese Patent Application P2002-352819
filed on December 4, 2002; the entire contents of which are
incorporated by reference herein.

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BACKGROUND OF THE INVENTION

1. Field of the Invention

15 The present invention relates to a reticle set used in
a double exposure process, and furthermore, a method of designing
the reticle set, a method of monitoring exposure using the reticle
set, a method of inspecting the reticle set, and a method of
manufacturing a semiconductor device.

2. Description of the Related Art

20 In recent years, a multiple exposure overlapping a
plurality of exposure processes for delineating a specific
pattern has attracted attention as one of different types of
micro-fabrication technologies. The performance of
semiconductor devices greatly depends on the dimensions of the
25 wiring pattern. Therefore, in a process using the multiple
exposure, it is required to control precisely parameters for

improving accuracy of the dimensions. In the case of using the multiple exposure, exposure conditions are usually determined for each exposure step, and each exposure step for a multiple exposure process is performed based on to conduct multiple exposure the determined exposure conditions.

In a photolithography process, a semiconductor circuit pattern is transferred by use of an aligner on a semiconductor substrate coated with a resist film. In forming a pattern by a reduction projection aligner, the resolution of the aligner is proportional to a wavelength λ of an exposure light and inversely proportional to a numerical aperture NA. Accordingly, responding to the demand of finer dimensions of semiconductor devices, the wavelength of the exposure light has been shortened, the NA of the projection lens has been increased, and process improvement associated therewith has been achieved. However, in order to achieve even finer dimensions of semiconductor devices required in recent years, it is more difficult to assure an exposure latitude and a depth of focus. Therefore, in order to effectively make use of the small exposure margin and improve accuracy of processed dimensions without causing a reduction in production yield, more accurate control of the exposure dose, i.e. the amount of exposure, and the focus is required.

As to the exposure dose control, an exposure dose monitoring method has been proposed. In this method, exposure is performed so as to have an inclined distribution of the exposure doses on a substrate, using a reticle set having patterns

therein with dimension ratios of transparent portions to opaque portions continuously changed in one direction by a pitch that cannot resolve images on the substrate by a reduction projection aligner (refer to Japanese Patent Laid-Open Application No. 5 2000-310850). Furthermore, as to the focus control, a method has been proposed in which focus is monitored using focus monitor patterns having a rhombus feature, that shift the exposure light in phase from each other to show different characteristics of pattern dimension for defocus (refer to Japanese Patent 10 Laid-Open Application No. 2001-100392).

As described above, in micro-fabrication it is important to control exposure conditions for photolithography with high accuracy in order to achieve processing accuracy and uniformity in pattern dimensions of semiconductor devices. Therefore, it 15 is necessary to provide many types of monitor marks such as an alignment mark, a dimension monitor mark, an exposure dose monitor mark and a focus monitor mark in the exposure area so that a large amount of data can be acquired and analyzed. However, in a reticle set on which a high density semiconductor circuit 20 pattern has been delineated, the monitor marks are disposed only in limited areas such as scribelines because of restrictions on layout. Accordingly, in an actual semiconductor integrated circuit manufacturing process, it is difficult to acquire detailed information on positions and dimensions over the entire 25 exposure area. As described above, currently used configuration of monitor marks are an obstacle to the improvement

of accuracy in micro-fabrication.

SUMMARY OF THE INVENTION

5 A first aspect of the present invention inheres in a reticle set including a first photomask having a circuit pattern provided with first and second openings provided adjacent to each other sandwiching a first opaque portion, and a monitor mark provided adjacent to the circuit pattern; and a second
10 photomask having a trim pattern provided with a second opaque portion configured to cover the first opaque portion in an area occupied by the circuit pattern and an extending portion connected to one end of the first opaque portion and configured to extend outside the area occupied by the circuit pattern
15 when the second photomask is aligned with a pattern delineated on a substrate by the first photomask.

 A second aspect of the present invention inheres in a method for designing a reticle set including forming in a first photomask, a circuit pattern having first and second openings
20 provided adjacent to each other sandwiching a first opaque portion, and a monitor mark adjacent to the circuit pattern; and forming in a second photomask, a trim pattern having a second opaque portion configured to cover the first opaque portion in an area occupied by the circuit pattern and an
25 extending portion connected to one end of the first opaque portion and configured to extend outside the area occupied

by the circuit pattern when the second photomask is aligned with a pattern delineated on a substrate by the first photomask.

5 A third aspect of the present invention inheres in an exposure monitoring method including delineating a wiring resist mask of a photoresist film by transferring a narrow line portion of a wiring of a circuit by a first exposure step; delineating a monitor resist pattern of the photoresist film by transferring an exposure monitor mark configured to measure
10 an exposure condition near the wiring resist mask at a position in an area where the wiring is to be delineated, the position being exposed by a second exposure step; and measuring the exposure condition for the first exposure step by the monitor resist pattern.

15 A fourth aspect of the present invention inheres in an inspection method for a reticle set including delineating a circuit pattern and an inspection monitor mark on a resist film coated on an opaque material film on a transparent substrate to form a resist mark; etching the opaque material
20 film by use of the resist mark to form a first photomask in which the circuit pattern has first and second openings provided adjacent to each other sandwiching a first opaque portion, and the inspection monitor mark provided adjacent to the circuit pattern; and inspecting the first photomask
25 by use of the inspection monitor mark.

A fifth aspect of the present invention inheres in a

manufacturing method for a semiconductor device including coating a first photoresist film on an underlying film on a semiconductor substrate; transferring a circuit pattern having first and second openings provided adjacent to each other sandwiching a first opaque portion and a monitor mark adjacent to the circuit pattern onto the first photoresist film from a first photomask by a first exposure step so as to delineate a wiring resist mask and a monitor resist pattern; selectively removing the underlying film by using the wiring resist mask and the monitor resist pattern as a mask so as to delineate a narrow line portion of a wiring of a circuit and a monitor underlying film; coating a second photoresist film on the semiconductor substrate on which the narrow line portion and the monitor underlying film is formed; delineating a trim resist mask by transferring a trim pattern from a second photomask onto the second photoresist film by a second exposure step, the trim pattern having a second opaque portion covering the first opaque portion in an area occupied by the circuit pattern, and an extending portion connected to one end of the first opaque portion and extending outside the area occupied by the circuit pattern; and delineating the wiring by selectively removing the monitor underlying film using the trim resist mask.

A sixth aspect of the present invention inheres in a manufacturing method for a semiconductor device including coating a photoresist film on a underlying film on a

semiconductor substrate; transferring a circuit pattern having first and second openings provided adjacent to each other sandwiching a first opaque portion and a monitor mark provided adjacent to the circuit pattern onto the photoresist film from a first photomask by a first exposure step so as to delineate a wiring resist latent image and a monitor resist latent image; projecting a trim pattern by a second exposure step from a second photomask onto the photoresist film exposed by the first exposure step, the trim pattern having a second opaque portion covering the first opaque portion in an area occupied by the circuit pattern, and an extending portion connected to one end of the first opaque portion and extending outside the area occupied by the circuit pattern; and delineating a wiring resist mask by a development process.

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BRIEF DESCRIPTION OF DRAWINGS

Figs. 1A and 1B are schematic views showing an example of a first photomask according to a first embodiment of the present invention;

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Figs. 2A and 2B are schematic views showing an example of a second photomask according to the first embodiment of the present invention;

Fig. 3 is a view showing an example of overlay of the first and second photomasks in a double exposure process according to the first embodiment of the present invention;

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Fig. 4 is a schematic view of an aligner used in explaining the double exposure process;

Figs. 5A and 5B are schematic views showing an example of a dimension monitor mark according to the first embodiment
5 of the present invention;

Figs. 6A and 6B are schematic views showing an example of an exposure dose monitor mark according to the first embodiment of the present invention;

Figs. 7 to 12 are examples of the cross-sectional views
10 for explaining the double exposure process according to the first embodiment of the present invention;

Fig. 13 is a schematic view showing an example of a wiring pattern formed by the double exposure process according to the first embodiment of the present invention;

Fig. 14 is a schematic view showing an example of a resist mask formed by a first exposure step of the double exposure process according to the first embodiment of the present
15 invention;

Fig. 15 is a schematic view showing an example of a first
20 photomask according to a second embodiment of the present invention;

Fig. 16 is a schematic view showing an example of a second photomask according to the second embodiment of the present invention;

Figs. 17A and 17B are schematic views showing an example of an alignment mark according to the second embodiment of the
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present invention;

Figs. 18 to 22 are examples of the cross-sectional views for explaining the double exposure process according to the second embodiment of the present invention;

5 Fig. 23 is a schematic view showing an example of a wiring pattern formed by the double exposure process according to the second embodiment of the present invention;

Figs. 24A and 24B are schematic views showing an example of a first photomask according to a third embodiment of the present invention;

10 Fig. 25 is a schematic view showing an example of a second photomask according to the third embodiment of the present invention;

Figs. 26A and 26B are schematic views showing an example of a transmittance monitor mark according to the third embodiment of the present invention; and

Figs. 27 to 32 are examples of the cross-sectional views for explaining the fabrication process for the first photomask according to the third embodiment of the present invention.

20 Fig. 33 is a graph showing an example of a distribution of a phase shift of the first photomask according to the third embodiment of the present invention.

25 DETAILED DESCRIPTION OF THE INVENTION

Various embodiments of the present invention will be

described with reference to the accompanying drawings. It is to be noted that the same or similar reference numerals are applied to the same or similar parts and elements throughout the drawings, and the description of the same or similar parts and elements will be omitted or simplified.

(FIRST EMBODIMENT)

For a multiple exposure according to a first embodiment of the present invention, a double exposure will be described where an alternating phase shift mask and a trim mask are used together. The double exposure includes exposing a circuit pattern by the alternating phase shift mask having a high resolution but having a restriction on a circuit layout and deleting an unnecessary pattern for the given circuit layout with a trim pattern.

In the reticle set according to the first embodiment of the present invention, alternating phase shift masks for printing circuit patterns 10a to 10c on a semiconductor wafer are disposed on a first photomask 5 configured to be used in a first exposure step as shown in Figs. 1A and 1B, and trim patterns 14a to 14c are disposed on a second photomask 6 configured to be used in the second exposure step as shown in Figs. 2A and 2B. In a corresponding area of the first photomask 5 on which another circuit pattern is scheduled to be printed on the semiconductor wafer in a later process, a monitor mark section 20 is also provided and includes various exposure monitor

marks.

The first photomask 5 has, as shown in Fig. 1A, an opaque film 9 shielding an exposure light, including a metal film such as chrome (Cr) or a metal compound film such as chrome oxide (Cr₂O₃) provided on the surface of a transparent substrate 3 of synthetic quartz and the like. For example, circuit patterns 10a to 10c, which may include gate wiring patterns of semiconductor devices have first rectangular shaped openings 11a to 11c, second rectangular shaped openings 12a to 12c, and first line shaped opaque portions 13a to 13c between the first openings 11a to 11c and the second openings 12a to 12c. A dimension monitor mark 21 configured to monitor the dimensions of exposed patterns, an exposure dose monitor mark 22 configured to monitor the exposure dose, and the like are arranged in the monitor mark section 20.

The circuit patterns 10a to 10c are alternating phase shift masks. As shown in Fig. 1B, which is a cross-sectional view taken along the line IB-IB of the first photomask 5 in Fig. 1A, in the circuit pattern 10a for example, the second opening 12a implemented by a trench in the transparent substrate 3 through the opaque film 9, shifts the phase by 180° relative to exposure light passing through the first opening 11a. Hence, when the first opaque portion 13a is transferred onto a semiconductor substrate by the exposure light transmitting the first opening 11a and the second opening 12a, diffracted light beams under the opaque portion 13a are canceled out, and thereby

the pattern is resolved on the semiconductor substrate. The dimension monitor mark 21 having opaque portions 21a to 21e, and the like, arranged as a lattice, are positioned near the circuit pattern 10a.

5 The second photomask 6, as shown in the plan view of Fig. 2A and the cross-sectional view of Fig. 2B, which is taken along the line IIB-IIB in Fig. 2A, has the trim patterns 14a to 14c of an opaque material film including a metal film such as Cr or a metal compound film such as Cr_2O_3 provided on the surface
10 of a transparent substrate 3a such as a synthetic quartz substrate. The trim patterns 14a to 14c respectively include extending portions 15a to 15c to be part of the wiring and second opaque portions 16a to 16c connected with the extending portions 15a to 15c. The pattern widths of the second opaque portions 16a
15 to 16c are designed to be sufficiently wider than the dimension of the resolution limit of an aligner. Here, the dimension of the resolution limit is expressed as $\lambda / \{ \text{NA} * (1 + \sigma) \}$, where λ is an exposure light wavelength, NA is a numerical aperture of a projection lens, and σ is a coherence factor of an
20 illumination optical system.

 An overlay of the first photomask 5 and the second photomask 6 will be described with reference to Fig. 3. As shown in Fig. 3, the first opaque portions 13a to 13c are aligned so as to be fitted to and covered by the second opaque portions 16a to
25 16c of the trim patterns 14a to 14c. The outer edges of the second opaque portions 16a to 16c are designed to be within

areas surrounded by the outer edges of the first and second openings 11a to 11c, and 12a to 12c of the circuit patterns 10a to 10c. Moreover, the extending portions 15a to 15c of the trim patterns 14a to 14c are designed to overlap respectively
5 with end lines of the first opaque portions 13a to 13c. The monitor mark section 20 including the dimension monitor mark 21, the exposure dose monitor mark 22, and the like is positioned near the circuit patterns 10a to 10c and the trim patterns 14a to 14c so as not to overlap the circuit patterns 10a to 10c
10 and the trim patterns 14a to 14c.

According to the reticle set of the first embodiment of the present invention, patterns formed on the semiconductor wafer by transferring the various exposure monitor marks positioned in the monitor mark section 20 in the first exposure
15 process are exposed and removed in the second exposure process. Therefore, on the first photomask 5, a large number of various exposure monitor marks can be positioned over the entire exposure area near the circuit patterns 10a to 10c with no restriction of the circuit layout. Thereby, detailed information of the
20 positions and dimensions in the entire exposure area on the semiconductor wafer where the semiconductor devices are fabricated can be acquired, so that exposure conditions can be controlled with high accuracy in the double exposure process.

An aligner 50 used in the description of the double exposure
25 process of the first embodiment of the present invention is a reduction projection aligner (stepper) having a reduction

ratio of 1/4 as shown in Fig. 4. A light source 41, a shutter 42, and an illumination lens system 44 implement an illumination optical system 40. A krypton fluoride (KrF) excimer laser having a wavelength λ of 248 nm, is used as the light source 41. The
5 illumination lens system 44 includes a fly eye lens and a condenser lens. A coherence factor σ representing the interference characteristic of the illumination optical system 40 is 0.75. A projection optical system 46 includes a projection lens and an aperture stop. The numerical aperture NA of the
10 projection lens is 0.68. By an exposure light B, the pattern of a reticle 4 of the reticle set provided between the illumination optical system 40 and the projection optical system 46 is demagnified and projected onto a semiconductor wafer (semiconductor substrate) 1 on a stage 48. The reticle 4 is
15 either the first photomask 5 or the second photomask 6. The reticle set can be implemented by, for example, a single reticle in which the first and second photomasks 5, 6 are disposed respectively in two divided areas of the reticle 4. Alternatively, the reticle set may have the first and second
20 photomasks 5, 6 disposed on respective transparent substrates. The exposure area per shot is about 23 by 30 mm square. Here, the "shot" is defined as a single event of light illumination to a predetermined exposure area on the substrate. While the reduction ratio of the aligner 50 is of 1/4 for the sake of
25 convenience in description, any reduction ratio can be used, as a matter of course. In the description below, the pattern

dimension on the reticle 4 will be described in terms of a dimension demagnified and projected on the semiconductor substrate 1 unless otherwise noted.

5 Next, various exposure monitor marks disposed in the monitor mark section 20 of the first photomask 5 will be described. The dimension monitor mark 21, as shown in the plan view of Fig. 5A and the cross-sectional view of Fig. 5B, has stripe-shaped opaque portions 21a to 21e having, for example, a length L_d of 1 μm and a width W_d of 110 nm arranged on the surface of the transparent substrate 3 at a pitch of 330 nm. A resist pattern, 10 formed by transferring the opaque portions 21a to 21e of the dimension monitor mark 21, is measured with a scanning electron microscope (SEM) and the like, to monitor transferred dimensions on a photoresist film.

15 The exposure dose monitor mark 22, as shown in the plan view of Fig. 6A and the cross-sectional view of Fig. 6B, is a diffraction grating where a plurality of opaque portions 22a to 22o on the transparent substrate 3 have a length L_e of 2 μm and widths W_e varying incrementally at a constant rate such that the opening ratio varies continuously. Here, the left ends 20 of the respective features are arranged periodically at a fixed pitch P_e of 190 nm. The opening ratio increases in the direction of both the right side and left side of the opaque film 22h at the center of the exposure dose monitor mark 22 in the drawing. 25 The opening ratio of the opaque film 22h at the center is 0%, and the opening ratios of the opaque films 22a and 22o at the

left and right ends are maximum and close to 100%. When the pitch P_e is not greater than the resolution limit of the aligner 50, the exposed diffraction grating pattern is not resolved on the semiconductor substrate 1. In the case of the aligner 50 (λ : 248 nm, NA: 0.68, σ : 0.75) used in the first embodiment of the present invention, the resolution limit is about 208 nm. Since the pitch P_e is not greater than the resolution limit, the patterns of the opaque portions 22a to 22o are not resolved. The intensities of the exposure light diffracted and passing between the opaque portions 22a to 22o vary with the opening rate. A resist pattern obtained by exposing the exposure dose monitor mark 22 has tilted sidewalls formed at the left and right ends of the exposure dose monitor mark 22 according to the sensitivity curve of the exposed photoresist film. Furthermore, the left and right ends of the exposure dose monitor mark 22 are demagnified according to the exposure dose so as to shrink the width. The exposure dose can be monitored using the amount of shrinkage of the pattern width obtained from measurement of the pattern width of the transferred exposure dose monitor mark 22.

In the double exposure process of the first embodiment of the present invention, the monitor mark section 20 including the exposure monitor marks such as the dimension monitor mark 21 and the exposure dose monitor mark 22 are disposed near the circuit patterns 10a to 10c of the first photomask 5. Moreover, transferred patterns of exposure monitor marks of the monitor

mark section 20, formed by being shielded from the light in the first exposure step are exposed through the second photomask 6 in the second exposure step. Hence, only a transferred pattern of the circuit patterns 10a to 10c shielded from the light by the trim patterns 14a to 14c of the second photomask 6 in the second exposure step is left. Therefore, on the first photomask 5, a large number of various exposure monitor marks can be provided over the entire exposure area near the circuit patterns 10a to 10c with no restriction on the layout of the circuit patterns. Thereby, detailed information on positions and dimensions over the entire exposure area where the semiconductor devices are formed can be acquired, so that exposure conditions can be controlled with high accuracy in the double exposure process.

Next, the double exposure process of the first embodiment of the present invention will be described using the cross-sectional view of Fig. 1B taken along the line IB-IB in Fig. 1A as an example, with reference to the cross-sectional views in Figs. 7 to 12.

(a) First, as shown in Fig. 7, an underlying film 35 such as a polysilicon film is deposited on a semiconductor substrate 1 to have a thickness of 200 nm, and a first positive-type photoresist film 36 is spin-coated on the underlying film 35 to have a thickness of 600 nm.

(b) In the first exposure step, a pattern of the first photomask 5 is projected onto the first photoresist film 36

on the surface of the semiconductor substrate 1 using the aligner 50 (see Fig. 4). After a development process, as shown in Fig. 8, a wiring resist mask 53a having a line feature sandwiched by the first and second resist opening portions 51a and 52a in resist masks 59 is delineated by transferring the circuit pattern 10a having the first and second openings 11a and 12a positioned adjacent to each other sandwiching the first opaque portion 13a in Fig. 1. Furthermore, the dimension monitor resist pattern 61 including the dimension monitor resist masks 61a to 61e is delineated by transferring the opaque portions 21a to 21e of the dimension monitor mark 21 shown in Figs 5A and 5B.

(c) Next, using the resist masks 59, a wiring resist mask 53a, and the dimension monitor resist masks 61a to 61e as masks, the underlying film 35 is selectively removed by an anisotropic reactive ion etching method (RIE) and the like, as shown in Fig. 9, to form underlying films 35a, a narrow line portion 7a of a wiring underlying film, and dimension monitor underlying film 71a to 71e.

(d) Subsequently, as shown in Fig. 10, a second positive-type photoresist film 37 is coated to have a thickness of 600 nm on the underlying films 35a, the narrow line portion 7a, and the dimension monitor underlying films 71a to 71e.

(e) In the second exposure step, a pattern of the second photomask 6 of Fig. 2 is projected onto the second photoresist film 37 using the aligner 50. As shown in Fig. 3, the projected

pattern of the second photomask 6 overlays the transferred pattern of the first photomask 5. The trim pattern 14a is transferred in an area occupied by the circuit pattern 10a of the first photomask 5. The trim pattern 14a has the second opaque portion 5 16a covering the first opaque portion 13a and the extending portion 15a overlapping one end of the first opaque portion 13a and extending outside the area occupied by the circuit pattern 10a. After a development process, as shown in Fig. 11, a trim resist mask 54 is delineated covering the narrow line portion 10 7a. Although not shown in Fig. 11, the trim resist mask 54 has a resist pattern formed thereon, corresponding to the extending portion 15a of the trim pattern 14a and connected with one end in the longitudinal direction of the narrow line portion 7a.

(f) Thereafter, the underlying film 35a is selectively 15 removed by RIE using the trim resist mask 54 as a mask. Here, since no resist mask is formed on the dimension monitor underlying film 71a to 71e, the narrow line portion 7a is left on the semiconductor substrate 1 as shown in Fig. 12. In Fig. 12, only the narrow line portion 7a delineated by transferring the circuit 20 pattern 10a is shown. However, other narrow line portions 7b, 7c delineated by transferring the circuit patterns 10b, 10c are also left on the semiconductor substrate 1.

By the above double exposure process, as shown in Fig. 13, an overlapping portion (see Fig. 3) of the patterns of the 25 first and second photomasks 5 and 6 is left on the semiconductor substrate 1 to delineate wirings 17a to 17c corresponding to

the gate electrodes of field effect transistors (FET), for example. The wirings 17a to 17c have respectively narrow line portions 7a to 7c corresponding to gate wirings, and wiring extending portions 8a to 8c connected to the respective ends
5 of the narrow line portions 7a to 7c and corresponding to contact portions for the gate wirings. The wiring extending portions 8a to 8c are delineated by selectively etching the underlying film 35a using a part of the trim resist mask 54 that is a resist pattern corresponding to the extending portion 15a of the trim
10 pattern 14a on the second photomask 6, as a mask. Because a resist pattern delineated by transferring the exposure monitor mark monitor mark section 20 is removed after the second exposure step, the monitor mark can be provided in an area where other wirings of a circuit are to be delineated in a later process.

15 In the monitoring method using the double exposure process of the first embodiment of the present invention, as shown in Fig. 14, the circuit patterns 10a to 10c are transferred in the first exposure step, and in the resist mask 59, the wiring resist masks 53a to 53c between the first and second resist
20 opening portions 51a to 51c and 52a to 52c are delineated. The dimension monitor resist pattern 61, an exposure dose monitor resist pattern 62, and the like are delineated by transferring the dimension monitor mark 21, the exposure dose monitor mark 22, and the like of the monitor mark section 20. The pattern
25 dimensions of the wiring resist masks 53a to 53c, the dimension monitor resist pattern 61, the exposure dose monitor resist

pattern 62, and the like are measured over the entire exposed area of the semiconductor substrate 1. For example, it is shown that the line width variation of the wiring resist masks 53a to 53c in the surface of the semiconductor substrate 1 depends
5 on the defocus variation based on comparison with the variations in the surface of the transferred resist pattern of the various monitor marks.

Thus, according to the first embodiment of the present invention, a large number of the various exposure monitor marks
10 can be provided over the entire exposure area near the circuit patterns 10a to 10c on the first photomask 5 with no restriction on layout of the circuit patterns. Thereby, detailed information on positions and dimensions over the entire exposure area where the semiconductor devices are fabricated can be
15 provided, so that exposure conditions can be controlled with high accuracy in the double exposure process.

(SECOND EMBODIMENT)

In a reticle set used for a double exposure according to
20 a second embodiment of the present invention, as shown in Figs. 15 and 16, alternating phase shift masks for printing circuit patterns 10d to 10f on a semiconductor wafer are provided on a first photomask 5a configured to be used in the first exposure step, and trim patterns 14d to 14f are provided on a second
25 photomask 6a configured to be used in the second exposure step. In a corresponding area of the first photomask 5a on which another

circuit pattern is scheduled to be printed on the semiconductor wafer in a later process, an alignment mark 25 is provided. The alignment mark 25 is disposed adjacent to the circuit patterns 10d to 10f of the first photomask 5a and the trim patterns 14d to 14f of the second photomask 6a so as not to overlap with the circuit patterns 10d to 10f and the trim patterns 14d to 14f. The reticle set according to the second embodiment is different from that of the first embodiment in that the alignment mark 25 is used as a monitor mark, and the rest of the configurations are the same as the first embodiment, and thus duplicated description is omitted.

As shown in Fig. 15, the circuit patterns 10d to 10f, which are patterns of, for example, gate wirings of semiconductor devices and provided on the first photomask 5a, have rectangular-shaped first openings 11d to 11f and second openings 12d to 12f that are provided on an opaque film 19, as well as line-shaped opaque portions 13d to 13f between the first openings 11d to 11f and the second openings 12d to 12f.

The second photomask 6a, as shown in Fig. 16, has trim patterns 14d to 14f made of an opaque material film provided on the surface of a transparent substrate 3c. The trim patterns 14d to 14f respectively include second opaque portions 16d to 16f which cover the opaque portions 13d to 13f in areas occupied by the circuit patterns 10d to 10f when aligned with the first photomask 5a, and extending portions 15d to 15f overlapping the respective ends of the opaque portions 13d to 13f and

extending outside the areas occupied by the circuit patterns 10d to 10f.

The alignment mark 25, as shown in the plan view of Fig. 17A and the cross-sectional view of Fig. 17B, has stripe-shaped opening portions 25a to 25i having, for example, a length L_a of 60 μm and a width W_a of 12 μm arranged at a pitch P_a of 24 μm on the opaque film 19 on the surface of a transparent substrate 3b. A resist pattern delineated by transferring the alignment mark 25 is detected by the aligner 50, so as to measure a displacement of the resist pattern caused by exposure conditions.

Next, the double exposure process of the second embodiment of the present invention will be described using a projected image corresponding to the line D-D of Fig. 15 as an example, with reference to the cross-sectional views in Figs. 18 to 22.

(a) First, as shown in Fig. 18, an underlying film 85 made of, for example, a polysilicon is deposited on a semiconductor substrate 1 to have a thickness of 200 nm, and a first positive-type photoresist film 86 is spin-coated on the underlying film 85 to have a thickness of 600 nm.

(b) In a first exposure step of the double exposure process, a pattern of the first photomask 5a is projected onto the photoresist film 86 on the surface of the semiconductor substrate 1 using the aligner 50 (see Fig. 4). As shown in Fig. 19, the circuit pattern 10d having the first and second openings 11d and 12d provided adjacent to each other sandwiching the first

opaque portion 13d in Fig. 15 is exposed, and a wiring resist latent image 81 is delineated sandwiched by exposed resist films 86a between unexposed resist portions 82. Furthermore, the opening portions 25a to 25i of the alignment mark 25 shown in
5 Figs. 17A and 17B are exposed, and alignment resist latent images 75a to 75d, corresponding to the opaque film 19 between the respective opening portions 25a to 25i, are delineated.

(c) Next, in the second exposure step, a pattern of the second photomask 6a is projected using the aligner 50 by detecting
10 the alignment resist latent images 75a to 75d. When aligned with the transferred patterns of the first photomask 5a, the entire surface is exposed except the wiring resist latent image 81, which was transferred by the first opaque portion 13, shielded by the trim pattern 14d having the second opaque portion 16d
15 and the extending portion 15d overlapping one end of the first opaque portion 13d and extending outside the area occupied by the circuit pattern 10d. Thus, an exposed resist film 86b is delineated as shown in Fig. 20.

(d) After a development process, as shown in Fig. 21, the
20 wiring resist latent image 81 is left on the underlying film 85 to delineate a wiring resist mask 83.

(e) Thereafter, the underlying film 85 is selectively removed by RIE using the wiring resist mask 83 as a mask. A narrow line portion 7d is delineated on the semiconductor
25 substrate 1 as shown in Fig. 22.

By the above-mentioned double exposure process, as shown

in Fig. 23, wirings 17d to 17f respectively having the narrow line portions 7d to 7f and wiring extending portions 8d to 8f corresponding to the extending portions 15d to 15f of the trim patterns 14d to 14f are delineated on the semiconductor substrate 1. Since the alignment resist latent images 75a to 75d delineated by transferring the opening portions 25a to 25i of the alignment mark 25 provided on the first photomask 5a are exposed in the second exposure step and removed in the development process, the alignment mark 25 can be provided in an area where another circuit pattern is scheduled to be printed in a later process.

In the monitoring method using the double exposure process according to the second embodiment of the present invention, in the first exposure step, the depolymerized exposed resist films 86a exposed through the opening portions 25a to 25i of the alignment mark 25 and the polymerized alignment resist latent images 75a to 75d are shielded from the light by the opaque film 19. The alignment resist latent images 75a to 75d can be optically detected because of differences in film thickness and optical characteristics such as the refraction index from the exposed resist films 86a. Immediately after the first exposure step, the alignment resist latent images 75a to 75d formed on the semiconductor substrate 1 using the first photomask 5a can be directly detected by the aligner 50, and displacements of the transferred alignment resist latent images 75a to 75d can be measured. Because the alignment mark 25 is

provided also in an area where another circuit pattern is scheduled to be printed on the semiconductor substrate 1 in a later process, the deviations can be measured in detail, so that the distortion of the exposure area on the semiconductor substrate 1 can be inspected. In the second embodiment of the present invention, the alignment mark 25 is used as a monitor mark. However, it may be possible to provide another monitor mark on the first photomask 5a, such as an exposure monitor mark for measuring an exposure condition using a monitor resist latent image delineated on a photoresist film in the first exposure step.

As described above, according to the second embodiment of the present invention, on the first photomask 5a, a large number of the exposure monitor marks can be provided over the entire exposure area near the circuit patterns 10d to 10f with no restriction on layout. Thereby, detailed information on positions and dimensions over the entire exposure area where the semiconductor devices are fabricated can be provided, so that exposure conditions can be controlled with high accuracy in the double exposure process.

(THIRD EMBODIMENT)

A method for inspecting a reticle set for the double exposure according to a third embodiment of the present invention is characterized in that a reticle set is easily fabricated and controlled with high accuracy by providing a monitor mark

for inspecting a photomask on a first photomask used in the first exposure step. The rest of the method is the same as the first and second embodiments, and thus duplicated description is omitted.

5 A first photomask 5b according to the third embodiment of the present invention, as shown in Fig. 24A, includes a circuit pattern 100 of an alternating phase shift mask, a phase shift monitor mark 26 for inspecting, for example, a photomask, and the like, which are arranged thereon. The circuit pattern 100
10 has a first opening 101 and a second opening 102 provided in an opaque film 99 and has a first linear opaque portion 103 between the first and second openings 101 and 102.

 As shown in the cross-sectional view of Fig. 24B, which is taken along the line XXVB-XXVB of the photomask 5b in Fig.
15 24A, in the circuit pattern 100 for example, in the second opening 102, a trench is formed through the opaque film 99 into the transparent substrate 3. The second opening 102 shifts the phase by 180° relative to exposure light passing through the first opening 101. Hence, when the first opaque portion 103 is
20 transferred onto a semiconductor substrate by the exposure light passing through the first and second openings 101 and 102, diffracted light under the opaque portion 103 is canceled out, and thereby the circuit pattern 100 is resolved on the semiconductor substrate 1. Positioned near the circuit pattern
25 100, for example, the phase shift monitor mark 26 having a trench with a square pattern with a length of each side of the square

being 4 μm is formed through the opaque film 99 into the transparent substrate 3.

5 The second photomask 6b used in the second exposure step, as shown in Fig. 25, has a trim pattern 104 made of a opaque material film provided on the surface of a transparent substrate 3e. The trim pattern 104 has a second opaque portion 106 covering the first opaque portion 103 in an area occupied by the circuit pattern 100 when aligned with the first photomask 5b, and an extending portion overlapping one end of the first opaque portion 103 and extending outside the area occupied by the circuit pattern 100.

15 The phase shift monitor mark 26, for example, as in the second opening 102, has the trench formed into the transparent substrate 3 so as to shift a phase by 180 degrees relative to the exposure light passing through the first opening portion 101. By measuring the phase of light passing through the phase shift monitor mark 26, the distribution of variations in phase in the first photomask 5b can be measured. Furthermore, for example, the dimension monitor mark 21 in Fig. 5, a transmittance 20 monitor mark 27 in Fig. 26A, and the like are disposed as a monitor mark for inspecting a photomask. The transmittance monitor mark 27, as shown in Fig. 26B, has a square opening in the opaque film 99 with each side having a length of 75 μm to measure the transmittance of a transparent substrate 3d to 25 the exposure light.

In the first photomask 5b according to the third embodiment

of the present invention, the inspection monitor marks for a photomask, such as the phase shift monitor mark 26 are provided adjacent to the circuit pattern 100 of the first photomask 5b and the trim pattern 104 of the second photomask 6b without
5 overlapping, in an area of the monitor marks including an area where another circuit pattern is to be placed in a later process. A pattern of the inspection monitor marks for a photomask transferred by shielding the exposure light by the first photomask 5b in the first exposure step is exposed through the
10 second photomask 6b in the second exposure step. Therefore, only the transferred pattern of the circuit pattern 100 shielded by the trim pattern 104 of the second photomask 6b in the second exposure step is left. Therefore, on the first photomask 5b, a large number of inspection monitor marks for a photomask can
15 be provided over the entire exposure area near the circuit pattern 100 with no restriction on layout of the circuit pattern. Thereby, detailed information on positions and dimensions information on the entire exposure area where the circuit pattern 100 is arranged can be acquired, so that the first photomask
20 5b, for highly accurately controlling exposure conditions in the double exposure process, can be accurately fabricated and controlled.

Next, the method of producing the first photomask 5b according to the third embodiment of the present invention will
25 be described with reference to the cross sectional views of Figs. 27 to 32.

(a) First, as shown in Fig. 27, a first resist film 91 is spin-coated on an opaque material film 98, such as a metal film of Cr and the like, deposited on the transparent substrate 3d made of synthetic quartz and the like.

5 (b) By use of an electron beam lithography system and the like, a circuit pattern of the first photomask 5b is delineated on the first resist film 91 according to pattern data. After a development process, as shown in Fig. 28, a first resist mask 91a corresponding to the circuit pattern of the first photomask
10 5b is delineated.

(c) Using the first resist mask 91a as a mask, the opaque material film 98 is selectively removed by RIE and the like, as shown in Fig. 29, to delineate the first opaque portion 103 sandwiched by the first opening 101 and an etching window 102a,
15 an etching window 26a and the transmittance monitor mark 27 in an opaque film 99.

(d) On the opaque film 99, on the transparent substrate 3d, as shown in Fig. 30, a second resist film 92 is coated.

(e) By use of an electron beam lithography system and the
20 like, opening patterns on the etching windows 102a and 26a are delineated on the first resist film 91 according to pattern data. After a development process, as shown in Fig. 31, a second resist mask 92a is delineated revealing the etching windows 102a and 26a expose.

25 (f) Thereafter, using the second resist mask 92a as a mask, the transparent substrate 3d is selectively removed by RIE,

etc., to delineate the second opening 102 and the phase shift monitor mark 26, in the transparent substrate 3d to a depth such that the phase of the exposure light is shifted by 180 degrees as shown in Fig. 32.

5 The phase and transmittance of a transmitted light are measured by an optical inspection apparatus using the inspection monitor marks for a photomask, such as the phase shift monitor mark 26 and the transmittance monitor mark 27 of the first photomask 5b fabricated in the above manner. Since the
10 inspection monitor marks for a photomask can be provided over the entire surface of the first photomask 5b, detailed control for the fabricated photomask is possible. It has been determined that, for example, the phase shift of the transmitted light measured with the phase shift monitor mark 26 has a concentric
15 distribution, as shown in Fig. 33, in the surface of the first photomask 5b having an area of 23 by 30 mm square. The concentric distribution of phase shift reflects the distribution of etched depth of the trenches in the transparent substrate 3d by RIE. This result is fed back into RIE etching conditions, so that
20 an alternating phase shift mask decreasing a phase shift distribution can be fabricated.

 According to the third embodiment of the present invention, on the first photomask 5b, a large number of the inspection monitor marks for a photomask can be provided over the entire
25 exposure area near the circuit pattern 100 with no restriction on layout of the circuit pattern. Thereby, detailed information

on positions and dimensions over the entire exposure area where the circuit pattern 100 is provided can be acquired, so that the first photomask 5b for highly accurately controlling exposure conditions in the double exposure process can be accurately fabricated and controlled.

(OTHER EMBODIMENTS)

In the first to third embodiments of the present invention, the reticle 4 is either the first photomask or the second photomask. For example, the reticle set may be a reticle set where the first and second photomasks are provided respectively in two divided areas of the reticle 4. Alternatively, the reticle set may be provided by the first and second photomasks respectively on individual transparent substrates as the reticle 4.

In the first and second embodiments of the present invention, a KrF excimer laser reduction projection aligner is used for the sake of convenience in the description. However, an ultraviolet light such as an i-line or g-line, another excimer, an electron beam, an X-ray, or the like can be used as a light source, as a matter of course.

Various modifications will become possible for those skilled in the art after receiving the teachings of the present disclosure without departing from the scope thereof.

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